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RESIN-SEALED SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEROF

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Abstract

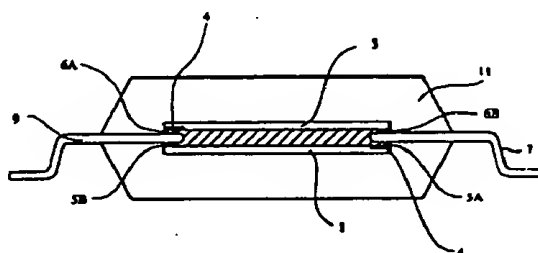
Purpose

The purpose is to provide a highly integrated semiconductor device with multiple semiconductor chips carried inside a single package.

Constitution

The invention provides a first semiconductor chip 1; a first insulation film formed on a first region of the surface of first semiconductor chip 1; a first bump 5A formed on the first insulation film; and a second bump 5B on the region of the surface of the first semiconductor substrate 1 [sic] where the first insulation film is not formed, and having a greater film

thickness than at least said first insulation film; a first lead 7 formed on top of the first bump 5A; a second lead 9 formed on top of the second bump 5B; a third bump 6A formed on top of the second lead 9; a second semiconductor chip 3 on which is formed a second insulation film on a second region above the third bump 6A; a fourth bump 6B between the first lead and the region on the second semiconductor chip 3 where the second insulation film is not formed; and an outer enclosure 11 around the periphery of the first semiconductor chip 1 and the second semiconductor chip 3.



Claims

1. Resin-sealed semiconductor device manufacturing method, characterized in that it includes a step in which a first insulation film is formed on the surface of a first semiconductor chip;

a step in which a desired region of the first insulation film is removed and a first bonding pad section is formed;

a step in which a first bump is formed on said first insulation film in at least the region where said first bonding pad section is not formed;

a step in which a second bump is formed, with a thickness greater than that of said first insulation film, on said first bonding pad section;

a step in which a second insulation film is formed on the surface of a second semiconductor chip;

a step in which a desired region of said second insulation film is removed and a second bonding pad section is formed;

a step in which a third bump is formed on said second insulation film in at least the region where said second bonding pad section is not formed;

a step in which a fourth bump is formed, with a thickness greater than that of said second insulation film, on said second bonding pad section;

a step in which said first semiconductor chip and said second semiconductor chip are aligned facing each other;

a step in which a first lead is connected sandwiched between said first bump and said fourth bump;

a step in which a second lead is connected sandwiched between said second bump and said third bump;

and a step in which said first semiconductor chip and said second semiconductor chip are resin sealed.

2. Resin-sealed semiconductor device manufacturing method of Claim 1, characterized in that said first bump is insulated from the circuit of said first semiconductor chip and said second bump conducts with the circuit of said first semiconductor chip, while said third bump is insulated from the circuit of said second semiconductor chip and said fourth bump conducts with the circuit of said second semiconductor chip.

3. Resin-sealed semiconductor device manufacturing method of Claim 1, characterized in that in the step in which resin sealing

is performed, the device that is formed utilizes a metal mold having a center gate.

4. Resin-sealed semiconductor device manufacturing method recorded Claim 1, characterized in that during the resin sealing step, resin fills the region between said first semiconductor chip and said second semiconductor chip.

5. Resin-sealed semiconductor device characterized in that it includes: a first semiconductor chip having on its surface a first insulation film, and a first bonding pad section in a desired region of this first insulation film; a first bump formed on said first bonding pad section of said first insulation film; a second bump formed on the surface of said first semiconductor chip in at least the region where there is no bonding pad section; a first lead connected above said first bump; a second lead connected above said second bump; a second semiconductor chip having on its surface a second insulation film, and a second bonding pad section in a desired region of this second insulation film; a third bump formed on said second bonding pad section of said second semiconductor chip and connected to said second lead; and a fourth bump, formed on the surface of said second semiconductor chip in at least the region where said second bonding pad section is not [formed], and connected to said first lead; an outer enclosure formed between said first semiconductor chip and said second semiconductor chip as well as around them.

6. Resin-sealed semiconductor device of Claim 5, characterized in that the height of said first bump is just equal to the thickness of said first insulation film and is greater than that of said second bump, and the height of said third bump is just equal to the thickness of said second insulation film and is greater than that of said fourth bump.

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